REMARKS

Claims 1-3, 5, 7-9, and 15 are presently pending and stand rejected under 35 U.S.C. § 103(a) as being obvious from U.S. Patent No. 6,310,921 ("Yoshioka") in view of U.S. Patent No. 5,706,059 ("Ran").

Claim 1 recites, among other limitations, "fetch reference pixels for a *first portion* of a picture" and "loads the memory controller with the *second portion* while the memory controller fetches the reference pixels".

Examiner has indicated that:

> Yoshioka teaches a video request manager [Fig. 3; Fig. 4; Fig. 16] comprising: a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; [Fig. 4; Fig. 16; Col. 11 Line 64 - Col. 12 Line 7; Col. 13 Line 56 - Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14] and a second state machine for commanding a memory controller to write a second portion of the picture [fig. 4; Col. 13 Line 56 - Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14, 20-27] memory controller fetches the reference pixels [Col. 14 Lines 38-45]
>
> Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem.

Office Action at 3-4.

In response to the previous Office Action, Assignee argued that Yoshioka does not teach "fetch reference pixels for a *first portion* of a picture" and "loads the memory controller with the *second portion*".

In response, the Office Action at 2 indicates that "Yoshioka reference was not cited by the Examiner as teaching 'fetch reference pixels for a first portion of a picture' and 'loads the memory controller with second

portion while the memory controller fetched the reference pixels".

Assignee understands that it is Examiner's position that "Ran teaches a memory is divided into several parts for processing and for loading reference pixels while processing is being performed".

However, Assignee maintains that Yoshioka does not teach "loads the memory controller with the *second portion*".

Assignee calls Examiner's attention to Yoshioka, Figure 4, and Col. 14, Lines 38-45, which was cited by Examiner as teaching "memory controller fetches the reference pixels".

> More specifically, for P-pictures or B-Pictures the pixel read/write unit 11 extracts a rectangle area indicated by the motion vector from the decoded reference frame in the external memory 3 via the memory controller 6 and blends the rectangle area with the block processed by the pixel calculation unit 10 to obtain an original block image. The decode result given by the pixel read/write unit 11 here is stored in the external memory 3 via the memory controller 6.

Note that "the pixel read/write unit 11 extracts a rectangle area" for the same block that "is stored in the external memory 3 via the memory controller 6". Therefore, the foregoing does not teach "fetch reference pixels for a *first portion* of a picture" and "loads the memory controller with the *second portion* while the memory controller fetches the reference pixels".

In Figure 10, Col. 18, Lines 6-27 (Emphasis Added)

> The read/write control unit 79 performs the MC on the block data inputted via the buffer 201 using the buffers A to D, and transfers the decoded images to the external memory 3 in units of two

blocks. More specifically, the read/write control unit 79 controls the memory controller 6 to read out rectangle areas corresponding to the present two blocks from the reference frame stored in the external memory 3 in accordance with the motion vectors set during the header analysis by the processor 7. As a result, the data of the rectangle areas corresponding to the two blocks indicated by the motion vectors are stored in the buffer A or the buffer B. Following this, the blending unit 76 performs the halfpel interpolation on the rectangle areas of the two blocks, depending on the picture type (whether the I-pictures, the P-pictures, or the B-pictures). The read/write control unit 79 calculates pixel values of the present two blocks by blending the block data inputted via buffer 201 with the halfpel interpolated rectangle areas (by adding the block data to the rectangle area), and then stores the calculated pixel values in the buffer B. These decoded blocks stored in the buffer B are transferred to the external memory 3 via the memory controller 6.

Note again, that the "read out rectangle areas" are for same block that is "transferred to the external memory 3". Therefore, Yoshioka does not teach "fetch reference pixels for a *first portion* of a picture" and "loads the memory controller with the *second portion* while the memory controller fetches the reference pixels".

Accordingly, Assignee respectfully traverses the rejection to claims 1 and 5 and requests that Examiner withdraw them, as well as dependent claims 2, 3, and 7-9 and 15.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

Mirut Dalal
Reg. No. 44,052
Attorney for Applicants

McAndrews, Held & Malloy, Ltd.
500 West Madison Street
Chicago, Illinois 60661

Telephone: (312) 775-8000
Facsimile: (312) 775-8100